breakdown protection diodes. The diodes may be oriented laterally or vertically within the transistor device. The orientation options may provide design flexibility for utilizing preexisting fabrication procedures to form and tune the diodes. The protection diodes are engineered to have a breakdown voltage slightly below the intrinsic breakdown voltage (BVdss) of the device to ensure breakdown always occurs at the protection diode. As described above, the breakdown voltage of the protection diodes may be tunable by adjusting the location, spacing, or dopant concentration levels of the regions defining the diode. With the drain and the isolating regions tied to one another, the drain voltage is clamped at the breakdown voltage of the protection diode. The transistor device may thus avoid entering the BVdss condition. With the protection diode spaced away from the normal current conduction path of the transistor device, the diode breakdown avoids causing destruction or degradation of device performance, such as the device I-V characteristics. With the integration of the protection diode, the size of the protection diode scales with the transistor device, thereby maintaining protection effectiveness when the width of the transistor device changes. These and other advantages may be achieved in a manner transparent to design and modeling. The protection diodes may be formed without any additional fabrication process steps, without any process modifications other than a mask layout change, and without any additional device footprint or area.

[0074] In a first aspect, a device includes a semiconductor substrate having a first conductivity type, a device isolating region in the semiconductor substrate, defining an active area, and having a second conductivity type, a body region in the active area and having the first conductivity type, and a drain region in the active area spaced from the body region to define a conduction path of the device, the drain region having the second conductivity type. The device isolating region and the body region are spaced from one another to establish a first breakdown voltage lower than a second breakdown voltage in the conduction path.

[0075] In a second aspect, an electronic apparatus includes a substrate having a first conductivity type, and a transistor disposed in the substrate. The transistor includes a first semiconductor region having a second conductivity type, a second semiconductor region having the first conductivity type, a third semiconductor region having the second conductivity type, adjacent the first semiconductor region, and spaced from the second semiconductor region by the first semiconductor region, and a fourth semiconductor region having the second conductivity type and defining an active area of the transistor in which the first, second and third semiconductor regions are disposed. The second and fourth semiconductor regions are configured to define a diode depletion region having a first breakdown voltage lower than a second breakdown voltage in the first semiconductor region.

[0076] In a third aspect, a method of fabricating a transistor includes forming a device isolating region of the transistor in a semiconductor substrate, the substrate having a first conductivity type, the device isolating region having a second conductivity type and defining an active area of the transistor, forming a body region of the transistor in the active area, the body region having the first conductivity type; and forming source and drain regions of the transistor in the active area, the source region being disposed on the body region, the source and drain regions having the second conductivity type. The device isolating region and the body region are spaced from one another to establish a first breakdown voltage lower than a second breakdown voltage in a conduction path between the source and drain regions.

[0077] Semiconductor devices with a conductive gate electrode positioned over a dielectric or other insulator may be considered MOS devices, despite the lack of a metal gate electrode and an oxide gate insulator. Accordingly, the terms metal-oxide-semiconductor and the abbreviation "MOS" may be used even though such devices may not employ metals or oxides but various combinations of conductive materials, e.g., metals, alloys, silicides, doped semiconductors, etc., instead of simple metals, and insulating materials other than oxides (e.g., nitrides, oxy-nitride mixtures, etc.). Thus, as used herein, the terms MOS and LDMOS are intended to include such variations.

[0078] The present invention is defined by the following claims and their equivalents, and nothing in this section should be taken as a limitation on those claims. Further aspects and advantages of the invention are discussed above in conjunction with the preferred embodiments and may be later claimed independently or in combination.

[0079] While the invention has been described above by reference to various embodiments, it should be understood that many changes and modifications may be made without departing from the scope of the invention. It is therefore intended that the foregoing detailed description be regarded as illustrative rather than limiting, and that it be understood that it is the following claims, including all equivalents, that are intended to define the spirit and scope of this invention.

1. A device comprising:

a semiconductor substrate having a first conductivity type;

a device isolating region in the semiconductor substrate, defining an active area, and having a second conductivity type;

a body region in the active area and having the first conductivity type; and

a drain region in the active area and spaced from the body region to define a conduction path of the device, the drain region having the second conductivity type;

wherein the device isolating region and the body region are spaced from one another to establish a first breakdown voltage lower than a second breakdown voltage in the conduction path.

2. The device of claim **1**, further comprising a source region in the active area and having the second conductivity type, wherein the body region comprises a first well on which the source region is disposed and a second well adjacent the first well and spaced from the device isolating region to establish the first breakdown voltage.

3. The device of claim **2**, wherein the first well and the second well have different dopant concentration levels.

4. The device of claim **1**, wherein the device isolating region comprises an isolation well configured as a ring surrounding the active area and spaced from the body region to establish the first breakdown voltage.

5. The device of claim **1**, wherein the device isolating region comprises a buried isolation layer in the semiconductor substrate, extending across the active area, and spaced from the body region to establish the first breakdown voltage.

6. The device of claim **1**, wherein the device isolating region comprises:

a well region in the semiconductor substrate and configured as a ring surrounding the active area;